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UTILITY APPLICATION FOR UNITED STATES PATENT  
FOR  
DELAY LOCKED LOOP DEVICE

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## DELAY LOCKED LOOP DEVICE

### Field of Invention

5       The present invention relates to a delay locked loop (DLL) device; and, more particularly, to a DLL device which synchronizes an internal clock signal with an external clock signal.

### 10   Description of Prior Art

      A delay locked loop (DLL) device is used for a synchronous semiconductor memory device to synchronize an internal clock signal with an external clock signal. Since  
15 there is a time delay while the external clock is inputted to the synchronous semiconductor memory device, the DLL device is needed for synchronizing the internal clock signal with the external clock signal.

      Fig. 1 is a block diagram showing a conventional DLL  
20 device disclosed in a commonly owned copending application, U.S. Ser. No. 10/331412, filed on Dec. 30, 2002, entitled "DIGITAL DLL APPARATUS FOR CORRECTING DUTY CYCLE AND METHOD THEREOF", which is incorporated herein by reference.

      The conventional DLL device includes a buffer 110, a  
25 delay line unit 120, a duty error control unit 130, a first delay model unit 140, a first direct phase detector 150, a second delay model unit 160 and a second direct phase detector

170.

The buffer 110 receives an external clock signal EXT\_CLK to output the inputted external clock signal as an input clock signal CLKI to the delay line unit 120. The delay line unit 120 receives and delays the input clock signal CLKI to output a first clock signal INTCLK1 after comparing a first comparative signal PD1 with the input clock signal CLKI; and to output a second clock signal INTCLK2 after comparing a second comparative signal PD2 with the input clock signal CLKI.

The duty error control unit 130 adjusts the first clock signal INTCLK1 and the second clock signal INTCLK2 by moving a falling edge of the first clock signal INTCLK1 and a falling edge of the second clock signal INTCLK2 into a middle of the two falling edges.

Thereafter, the duty error control unit 130 outputs the adjusted first clock signal as a first mixed clock signal INT\_CLK, and outputs the adjusted second clock signal as a second mixed clock signal INTCLK2. The first delay model unit 140 receives the first mixed clock signal INT\_CLK and estimates a delay amount generated while the first mixed clock signal INT\_CLK travels to a data input/output pin (DQ pin). Then, the first delay model unit 140 generates a first compensated clock signal ICLK1 based on the estimated delay amount.

The first direct phase detector 150 outputs the first comparative signal PD1 to the delay line unit 120 after comparing the external clock signal EXT\_CLK with the first

compensated clock signal ICLK1.

The second delay model unit 160 receives the second mixed clock signal INTCLK2 and estimates a delay amount generated while the second mixed clock signal INTCLK2 travels to a data input-output pin (DQ pin). Then, the second delay model unit 160 generates a second compensated clock signal ICLK2.

However, the conventional DLL device has a power consuming problem because two phase mixers (not shown), the two delay model units (140 and 160) and the two direct phase detectors (150 and 170) continue to operate after a delay value of the conventional DLL is locked. In addition, since both the two delay lines continue to operate after the DLL is locked, a total phase error of the DLL device is equal to a phase error of one of the two delay lines.

#### Summary of Invention

It is, therefore, an object of the present invention to provide a DLL device that consumes less power, and has low jitter characteristic.

In accordance with an aspect of the present invention, there is provided a DLL device including a first delay line for receiving an external clock signal and a first delay control signal to generate a first internal clock signal; a second delay line for receiving the external clock signal and a second delay control signal or the first delay control

signal to generate a second internal clock signal; a first delay control block for receiving the external clock signal to generate the first delay control signal; a second delay control block for receiving the external clock signal to generate the second delay control signal; and a phase detecting block for receiving the first internal clock signal and the second internal clock signal to generate the on-off signal by comparing a phase of the first internal clock signal with a phase of the second internal clock signal.

#### Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a conventional delay locked loop (DLL) device;

Fig. 2 is a block diagram showing a DLL device in accordance with the present invention;

Fig. 3 is a timing diagram showing an operation of the DLL device in accordance with the present invention;

Fig. 4 is a block diagram showing delay lines included in the DLL device in accordance with the present invention;

and

Figs. 5A and 5B show sample processes of controlling the delay lines shown in Fig. 4.

## Detailed Description of Invention

Hereinafter, a delay locked loop (DLL) device in accordance with the present invention will be described in detail referring to the accompanying drawings.

Fig. 2 is a block diagram showing the DLL device in accordance with the present invention.

As shown, the DLL device includes a buffer 210, a delay line unit 220, a phase detector 230, a mixing controller 240, a first delay control block 250 and a second delay control block 260.

The buffer 210 receives an external clock signal EXT\_CLK to output an input clock signal ECLK to the delay line unit 220.

The delay line unit 220 includes a first delay line 221 and a second delay line 222. The 220 receives the input clock signal ECLK from the buffer 210, a first comparative signal PD1 from the first delay control block 250 and a second comparative signal PD2 from the second delay control block 260.

The first delay line 221 included in the delay line unit 220 receives the input clock signal ECLK and the first comparative signal PD1; and, then, the first delay line 221 delays the input clock signal ECLK depending on the first comparative signal PD1 to output a first clock signal INTCLK1 to the first delay control block 250.

The second delay line 222 included in the delay line unit 220 receives the input clock signal ECLK and the second

comparative signal PD2; and, then, the second delay line 222 delays and inverts the clock input signal ECLK depending on the second comparative signal PD2 to output a second clock signal INTCLK2 to the second delay control block 260.

5       The phase detector 230 receives the first clock signal INTCLK1 and the second clock signal INTCLK2 from the delay line unit 220. Then, the phase detector 230 generates a phase detecting signal, where the phase detecting signal indicates which of the two falling edges of the first clock signal  
10 INTCLK1 and the second clock signal INTCLK2 leads; and, then, the phase detecting signal is inputted to the mixing controller 240.

      The mixing controller 240 determines whether the DLL is locked or not, and outputs a weight value K to the first delay  
15 control block 250 and the second delay control block 260. The mixing controller 240 also generates an on-off signal ON\_OFF which is determined by whether the DLL is lock or not, and outputs the on-off signal ON\_OFF to the second delay control block 260. The weight value K is determined by the phase  
20 detecting signal.

      The first phase mixer 251 included in the first delay control block 250 generates a first mixed clock signal INT\_CLK after adjusting duties of the first and second clock signals INTCLK1 and INTCLK2 by applying the weight value 1-K to the  
25 first clock signal INTCLK1 and the weight value K to the second clock signal INTCLK2.

      The first delay model 252 included in the first delay

control block 250 receives the first mixed clock signal INT\_CLK from the first phase mixer 251 to generate the first compensated clock signal ICLK1 after compensating time difference between the external clock signal EXT\_CLK and the  
5 first mixed clock signal INT\_CLK.

The first direct phase detector 253 included in the first delay control block 250 receives the external clock signal EXT\_CLK and the first compensated clock signal ICLK1, and generates the first comparative signal PD1 after comparing  
10 the external clock signal EXT\_CLK with the first compensated clock signal ICLK1.

The second delay control block 260 generates a second compensated clock signal ICLK2 from the received signals, the weight value K, the first clock signal INTCLK1 and the second  
15 clock signal INTCLK2. The second delay control block 260 also receives the external clock signal EXT\_CLK, and generates the second comparative signal PD2 after comparing the external clock signal EXT\_CLK with the second compensated clock signal ICLK2. The second delay control block 260 becomes activated  
20 or inactivated depending on the on-off signal ON\_OFF.

The second phase mixer 261 included in the second delay control block 260 generates a second mixed clock signal INTCLK2' after adjusting duties of the first and second clock signals INTCLK1 and INTCLK2 by applying the weight value K to  
25 the first clock signal INTCLK1 and the weight value 1-K to the second clock signal INTCLK2. The second phase mixer 261 becomes enabled or disabled depending on the on-off signal



ON\_OFF.

The second delay model unit 262 included in the second delay control block 260 receives the second mixed clock signal INTCLK2' from the second phase mixer 261, and generates the second compensated clock signal ICLK2 after compensating time difference between the external clock signal EXT\_CLK and the second mixed clock signal INTCLK2'. The second delay model unit 262 becomes enabled or disabled depending on the on-off signal ON\_OFF.

The second direct phase detector 263 included in the second delay control block 260 receives the external clock signal EXT\_CLK and the second compensated clock signal ICLK2, and generates the second comparative signal PD2 after comparing the external clock signal EXT\_CLK with the first compensated clock signal ICLK1. The second direct phase detector 263 becomes enabled or disabled depending on the on-off signal ON\_OFF.

Fig. 3 is a timing diagram showing an operation of the DLL device in accordance with the present invention.

If the DLL is locked, rising edges of the first compensated clock signal ICLK1 and the second compensated clock signal ICLK2 become in phase; and, rising edges of the first clock signal INTCLK1, the second clock signal INTCLK2, the first mixed clock signal INT\_CLK and the second mixed clock signal INTCLK2' become in phase. Herein, if the DLL is locked, the second direct phase detector 263 is turned off, and only the first direct phase detector 253 controls both the

first delay line 221 and the second delay line 222 included in the delay line unit 220.

For example, if a rising edge of the first mixed clock signal INT\_CLK lags behind a rising edge of the external clock signal EXT\_CLK, the first direct phase detector 253 commands the first delay line 221 and the second delay line 222 to reduce delay quantity. Therefore, rising edges of the first clock signal INTCLK1 and the second clock signal INTCLK2 are advanced; and, consequently, the rising edge of the first mixed clock signal INT\_CLK is also advanced.

Therefore, when the DLL device starts to operate, both the first delay line 221 and the second delay line 222 operate being controlled by the first direct phase detector 253 and the second direct phase detector 263. However, once the DLL is locked, only the first direct phase detector 253 operates controlling both the first delay line 221 and the second delay line 222.

Therefore, the second phase mixer 261, the second delay model unit 262 and the second direct phase detector 263 can be turned off, and the DLL device can save power.

Fig. 4 is a block diagram of the first delay line 221 and the second delay line 222.

A first delay control unit 411 included in the first delay line 221 receives the first comparative signal PD1 from the first direct phase detector 253, and generates a first delay control signal UPDN1 and a first delay enable signal DL1\_EN.

A first coarse delay line 412 included in the first delay line 221 is activated by the first delay enable signal DL1\_EN, and controls delay of the clock input signal ECLK depending on the first delay control signal UPDN1.

5        A first fine delay line 413 included in the first delay line 221 is activated by the first delay enable signal DL1\_EN, and generates the first clock signal INTCLK1 by delaying an outputted signal from the first coarse delay line 412 depending on the first delay control signal UPDN1.

10       A second delay control unit 421 included in the second delay line 222 receives the second comparative signal PD2 from the second direct phase detector 263, and generates a second delay control signal UPDN2 and a second delay enable signal DL2\_EN. If the DLL is locked, the second delay control unit  
15       421 receives the first delay enable signal DL1\_EN and the first delay control signal UPDN1 from the first delay control unit 411, and outputs the second delay enable signal DL2\_EN and the second delay control signal UPDN2.

20       A second coarse delay line 422 included in the second delay line 222 is activated by the second delay enable signal DL2\_EN, and controls delay of the clock input signal ECLK depending on the second delay control signal UPDN2.

25       A second fine delay line 423 included in the second delay line 222 is activated by the second delay enable signal DL2\_EN, and generates the second clock signal INTCLK2 by delaying an outputted signal from the second coarse delay line 422 depending on the second delay control signal UPDN2.

The following Table. 1 shows operation of the first delay line 221 and the second delay line 222.

Table. 1

	Previous  first  comparative  signal PD1	Current  first  comparative  signal PD1	Second  comparative  signal  PD2	First  delay  enable  signal  DL1_EN	Second  delay  enable  signal  DL2_EN	First delay  control  signal  UPDN1	Second  delay  control  signal  UPDN2
Before  the DLL  is  locked	x	First value	Second  value	Logic  High	Logic  High	First value	Second  value
After  the DLL  is  locked	Previous first  comparative signal =  current first  comparative signal		x	Previously logic  Low signal  becomes logic  High		Current  first  comparative  signal PD1	Current  first  comparative  signal PD1
	/Previous first  comparative signal =  current first  comparative signal			Previously logic  High signal  becomes logic  High			

5        The first delay enable signal DL1\_EN controls the first delay line 221 to operate delay tuning, and the second delay enable signal DL2\_EN controls the second delay line 222 to operate delay tuning.

10       After the DLL device is locked, one of the first enable signal DL1\_EN and the second enable signal DL2\_EN becomes a

logic 'HIGH' level depending on values of a previous first comparative signal PD1 and a current first comparative signal PD1. If the current first comparative signal PD1 is an Nth outputted signal, the previous first comparative signal PD1 is an (N-1)th outputted signal, where N is a natural number bigger than one. If the current first comparative signal PD1 is equal to the previous first comparative signal PD1, one of the first delay enable signal DL1\_EN and the second delay enable signal DL2\_EN becomes a logic 'HIGH' level and the other signal becomes a logic 'LOW' level, wherein a previous state of the signal which changed as a logic 'HIGH' level is a logic 'LOW' level. If the current first comparative signal PD1 is different from the previous first comparative signal PD1, previous values of the first delay signal DL1\_EN and the second delay signal DL2\_EN become current values, i.e., previously logic 'HIGH' level signal becomes a logic 'HIGH' level, and previously logic 'LOW' signal becomes a logic 'LOW' level.

Therefore, it is possible to synchronize the first clock signal INTCLK1 with the second clock signal INTCLK2 by using the above method.

Low jitter characteristic is also achieved by using the above method, and the reason why is described below.

Each of the first delay line 221 and the second delay line 222 has a phase step size, where the phase step size is the minimum size the two delay lines 221 and 222 can tune delay, i.e., the two delay lines 221 and 222 can not delay a

clock signal less than the phase step size.

If the phase step size is  $TUD$ , each of the first delay line 221 and the second delay line 222 has a phase error of  $\pm TUD$ .

5        Therefore, if both the first delay line 221 and the second delay line 222 operate simultaneously, the first mixed clock signal INT\_CLK has a phase error of  $\pm TUD$  at the worst case.

10       However, if the two delay lines operate by turns, the first mixed clock signal INT\_CLK has a phase error of  $\pm TUD/2$  at the worst case. Therefore, the low jitter characteristic can be achieved.

15       Fig. 5A and 5B show sample processes of controlling the two delay line, the first delay line 221 and the second delay line 222, after the DLL is locked.

Referring to Fig. 5A, if a rising edge of the first mixed clock signal INT\_CLK leads a rising edge of the external clock signal EXT\_CLK after the  $(N-1)$ th delay tuning, the first comparative signal PD1 commands a more delay. By the command of the first comparative signal PD1, the second clock signal INTCLK2 is delayed for  $tUD$ , where  $tUD$  is a phase step size that the first fine delay line 413 and the second fine delay line 423 have. Thereafter, if a rising edge of the first mixed clock signal INT\_CLK lags behind a rising edge of the external clock signal EXT\_CLK after the  $N$ th delay tuning, the first comparative signal PD1 commands a less delay. Because the current first comparative signal PD1 is different from the

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previous first comparative signal PD1, the second clock signal INTCLK2 is controlled by the command again.

Referring to Fig. 5B, if a rising edge of the first mixed clock signal INT\_CLK leads a rising edge of the external clock signal EXT\_CLK after the (N-1)th delay tuning, the first comparative signal PD1 commands a more delay. By the command of the first comparative signal PD1, the second clock signal INTCLK2 is delayed for tUD. However, in this case, a rising edge of the first clock signal INT\_CLK still leads a rising edge of the external clock signal EXT\_CLK after the Nth delay. Therefore, the first comparative signal commands a more delay again. Because, in this case, the current first comparative signal PD1 is equal to the previous first comparative signal PD1, the first INTCLK1 is controlled by the command.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.